

IT IS CLAIMED:

1. A non-volatile memory comprising:
  - an array of non-volatile storage units arranged into a plurality of bit lines and forming one or more rows;
  - a data transfer line;
  - a plurality of data transfer circuits each connectable to a respective set of one or more of the bit lines and the data transfer line to transfer data between the respective set of bit lines and the data transfer line, wherein data is transferred between each of the data transfer circuits and the data transfer line in response to a respective column select signal; and
  - a plurality of column select circuits connected to form a clocked shift register, having a clock input, each connected to a respective data transfer circuit to provide the respective column select signal, and each having a fuse input, wherein when a fuse signal is asserted on the fuse input, the column select circuit passes the shift register pulse to next stage in the shift register without waiting for the clock and without asserting its respective column select signal.
2. The non-volatile memory of claim 1, wherein each of the data transfer circuits comprises:
  - a set of one or more temporary data storage unit to store data transferred between the respective set of bit lines and the data transfer line.
3. The non-volatile memory of claim 2, wherein each of the data transfer circuits further comprises:
  - a output circuit connectable to the data transfer line in response to the respective column select signal, wherein the set of said temporary data storage units are a plurality and wherein the output circuit can randomly access each of said plurality of temporary data storage units.
4. The non-volatile memory of claim 3, wherein each of the data transfer circuits further comprises:
  - a plurality of sense amplifiers, wherein the respective set of bit lines is a plurality and the number of said sense amplifiers is the same as the

number of bit lines in said respective set and wherein each bit line can randomly access each of said plurality of temporary data storage units through a corresponding one of the sense amplifiers.

5. The non-volatile memory of claim 2, wherein each of the data transfer circuits further comprises:

a output circuit, wherein the set of said temporary data storage units are a plurality connected in a first in, first out manner with the last of the temporary data storage units connected to the output circuit and the corresponding set of bit lines are connectable to the first of the temporary data storage units, and wherein the output circuit is connectable to the data transfer line in response to the respective column select signal.

6. The non-volatile memory of claim 5, wherein each of the data transfer circuits further comprises:

a plurality of sense amplifiers, wherein the respective set of bit lines is a plurality and the number of said sense amplifiers is the same as the number of bit lines in said respective set and wherein each bit line is connectable to the first of the temporary data storage units through a corresponding one of the sense amplifiers.

7. The non-volatile memory of claim 6, wherein for each of said data transfer circuits, the number said temporary data storage units in the set is a multiple of the number of bit lines in the corresponding set of bit lines.

8. The non-volatile memory of claim 7, wherein said non-volatile storage units each can store  $N$  bits of data and the ratio of the number of temporary data storage units to the number of bit lines is  $N$ , wherein  $N$  is an integer greater than or equal to one.

9. The non-volatile memory of claim 2, wherein each of the data transfer circuits further comprises:

an input circuit, wherein the set of said temporary data storage units are a plurality connected in a first in, first out manner connected to the input circuit and the corresponding set of bit lines are connectable to the first of the

temporary data storage units, and wherein the input circuit is connectable to the data transfer line in response to the respective column select signal.

10. The non-volatile memory of claim 1, wherein each of said column select circuits comprises:

a master register and a slave register, wherein said column select signal is asserted in response the output of the slave register when the fuse signal is de-asserted.

11. The non-volatile memory of claim 10, wherein each of said column select circuits comprises:

a master register and a slave register, wherein said column select signal is asserted in response to the output of the slave register when the fuse signal is de-asserted.

12. The non-volatile memory of claim 11, wherein in response to the fuse signal being asserted in a respective column select circuit, the corresponding master and slave registers are each converted into unclocked buffers or inverters.

13. The non-volatile memory of claim 1, further comprising:

a ROM memory portion containing bad column information, wherein the fuse signals are determined from said bad column information.

14. The non-volatile memory of claim 13, wherein the fuse signals are determined by the memory at power up.

15. The non-volatile memory of claim 1, wherein each of said shift registers is connected to receive a directional control signal, and wherein when the directional control signal is asserted in the shift register each of said column select circuits is connected to receive the shift register input from the adjacent shift register to its left and when the directional control signal is de-asserted in the shift register each of said column select circuits is connected to receive the shift register input from the adjacent shift register to its right.

16. A memory system circuit, comprising:

a controller; and

a memory comprising one or more independently controllable non-volatile data storage sections connected to the controller, wherein each of said storage sections comprises:

an array of non-volatile user data storage units arranged in rows and columns;

a memory portion containing bad column information; and

column select circuitry connected to the array and the memory portion containing bad column information, wherein bad columns are replaced based on the bad column information in a manner transparent to the controller.

17. The memory system circuit of claim 16, wherein the user data storage units are multi-state storage units.

18. An integrated circuit comprising:

a plurality of nonvolatile storage units arranged in rows and columns;

a plurality of programming circuits coupled to the columns of storage units;

a plurality of sense amplifiers coupled to the columns of storage units;

a plurality of latch circuits able to temporarily store data, coupled to either the programming or sensing circuits, or to both;

a plurality of input circuits coupled to the storage units;

a plurality of output circuits coupled to the storage units

a ROM memory storing bad column information; and

a shift register comprising a plurality of pointer shift register stages coupled to the ROM memory portion, wherein each stage has a clock input and is coupled to an enable stage of either one or some of the programming, sensing, data storage, input and/or output circuits except for those stages corresponding to a bad column as identified by the bad column information.

19. The integrated circuit of claim 18 wherein the memory cells are floating gate, Flash, EEPROM, or EPROM memory cells.

20. The integrated circuit of claim 18 wherein each stage of the shift register comprises a master-slave register.

21. The integrated circuit of claim 18 wherein the storage unit stores are multistate memory cells.

22. The integrated circuit of claim 18 wherein combinations of multiple latch circuits can be assigned to store multiple bits of information.

23. A method of operating an integrated circuit comprising:  
providing a plurality of latches to hold data associated with a respective one of a plurality of columns of memory cells;  
providing a shift register having a plurality of stages with an output coupled to an enable input of a respective latch;  
fusing out one or more of the shift register stages;  
loading a strobe bit into a first stage of the shift register to enable coupling of the corresponding first latch to an input line; and  
clocking the shift register to advance the strobe bit from the first stage of the shift register to the subsequent stages to enable coupling of the corresponding subsequent latches to the input line, wherein when a stage is fused out the strobe bit is advanced through the fused out stage without being clocked and without the fused out stage enabling the corresponding latch to an input line.

24. The method of claim 23, wherein the memory cells are multi-state memory cells.

25. The method of claim 23, further comprising:  
reading a memory portion on the integrated circuit, wherein said fusing out one or more of the shift registers is based on the contents of said memory portion.

26. The method of claim 23, further comprising:  
asserting a control signal to the shift register when the strobe bit reaches the last stage of the shift register, wherein in response to the control signal the shift register advances the strobe bit from the last stage of the shift register to the preceding stages.